CLAIM AMENDMENTS

1. (original) A semiconductor switch circuit comprising:

a first semiconductor switch, a second semiconductor switch, and a third semiconductor switch inserted between an input terminal and an output terminal and connected in series;

first and second voltage application means connected in parallel to the first semiconductor switch, one end of which is connected to said input terminal and the other end is connected to one end of the second semiconductor switch, and to the third semiconductor switch, one end of which is connected to the other end of the second semiconductor switch and the other end is connected to said output terminal; and

switch control means for operating and controlling said first semiconductor switch, second semiconductor switch, and third semiconductor switch in the ON and OFF states, and simultaneously operating and controlling the first and second voltage application means in the OFF and ON states in a reverse mode;

wherein when said first semiconductor switch, second semiconductor switch, and third semiconductor switch are operated and controlled in the OFF state by the switch control means, said first and second voltage application means are each controlled to the ON state, the first voltage application means applies the potential of the input terminal to a first voltage application point that is the junction between said first semiconductor switch and second semiconductor switch, and the second voltage application means applies the potential of the output terminal to a second voltage application point that is the junction between said second semiconductor switch and third semiconductor switch.

2. (original) A semiconductor switch circuit comprising:

at least two semiconductor switches inserted between an input terminal and an output terminal and connected to each other in series;

voltage application means connected in parallel to either one of said two semiconductor switches; and

switch control means for operating and controlling said two semiconductor switches in the ON state and OFF state, and simultaneously controlling said voltage application means in the OFF state and ON state in a reverse mode;

wherein when said two semiconductor switches are operated and controlled in the OFF state by the switch control means, said voltage application means is controlled to the ON state, and applies to a voltage application point that is the junction of said two semiconductor switches the potential of the input terminal or output terminal to which said one of the semiconductor switches that is connected in parallel to the voltage application means is connected.

3. (original) The semiconductor switch circuit according to claim 1 or 2, wherein said voltage application means comprises:

a direct current amplifier set to a gain state of approximately +1; and

a voltage application semiconductor switch connected between the output terminal of the direct current amplifier and the voltage application point, for operating in a reverse mode with said semiconductor switches.

4. (original) The semiconductor switch circuit according to claim 1 or 2, wherein said voltage application means comprises:

a direct current amplifier set to a gain state of approximately +1; and

a resistor connected between the output terminal of the direct current amplifier and the voltage application point.

5. (original) The semiconductor switch circuit according to claim 1 or 2, wherein said semiconductor switch that is connected in parallel to the voltage application means comprises anti-parallel connected diode elements.

6. (previously presented) A matrix circuit comprising:

a plurality of input terminals;

a plurality of output terminals; and

a plurality of semiconductor switches arranged in matrix form between the input terminals on one side and the output terminals on the other side of a matrix circuit; wherein the semiconductor switch circuit according to claim 1 or 2 is used as said semiconductor switches arranged in matrix form in the matrix circuit.

7. (currently amended) A semiconductor device testing apparatus including a matrix circuit in which the semiconductor switch circuit according to claim 1 or 2 is used, whereby a plurality of voltage/current generators ~~can be~~ are connected to a plurality of terminal pins of a semiconductor device under test by means of said matrix circuit.

8. (previously presented) A matrix circuit comprising:

a plurality of input terminals;

a plurality of output terminals; and

a plurality of semiconductor switches arranged in matrix form between the input terminals on one side and the output terminals on the other side of a matrix circuit; wherein the semiconductor switch circuit according to claim 3 is used as said semiconductor switches arranged in matrix form in the matrix circuit.

9. (previously presented) A matrix circuit comprising:

a plurality of input terminals;

a plurality of output terminals; and

a plurality of semiconductor switches arranged in matrix form between the input terminals on one side and the output terminals on the other side of a matrix circuit; wherein the semiconductor switch circuit according to claim 4 is used as said semiconductor switches arranged in matrix form in the matrix circuit.

10. (previously presented) A matrix circuit comprising:

a plurality of input terminals;

a plurality of output terminals; and

a plurality of semiconductor switches arranged in matrix form between the input terminals on one side and the output terminals on the other side of a matrix circuit; wherein the semiconductor switch circuit according to claim 5 is used as said semiconductor switches arranged in matrix form in the matrix circuit.

11. (currently amended) A semiconductor device testing apparatus including a matrix circuit in which the semiconductor switch circuit according to claim 3 is used, whereby a plurality of voltage/current generators ~~can be~~ are connected to a plurality of terminal pins of a semiconductor device under test by means of said matrix circuit.

12. (currently amended) A semiconductor device testing apparatus including a matrix circuit in which the semiconductor switch circuit according to claim 4 is used, whereby a plurality of voltage/current generators ~~can be~~ are connected to a plurality of terminal pins of a semiconductor device under test by means of said matrix circuit.

13. (currently amended) A semiconductor device testing apparatus including a matrix circuit in which the semiconductor switch circuit according to claim 5 is used, whereby a plurality of voltage/current generators ~~can be~~ are connected to a plurality of terminal pins of a semiconductor device under test by means of said matrix circuit.